Agilent EEsof EDA

High Speed Digital Design with Advanced Design System

Agilent Technologies

Jump the Gigabit-per-Second Barrier

Today's high-speed digital designers require EDA tools that accurately model RF and microwave effects, and that analyze not only signal integrity, but also the power integrity, EMC, and EMI of serial and parallel chip-to-chip data links. A prime example is signal integrity on serial links.

Increasing consumer and business demand for digital entertainment and information transmission is driving the need for high-speed systems such as routers, servers, mass storage system, and PCs. Chip-to-chip connections inside these systems have undergone an architectural shift from parallel busses to serializer/deserializer (SERDES) links. Such serial links eliminate parallel bus clock skew and reduce the number of traces — advantages that come at the cost of large increases in bit rate on the remaining traces. At data rates greater than a gigabit per second and with channel flight times longer than a bit period, signal integrity is a major concern. Under these conditions, high-speed analog effects, previously only seen in high-frequency RF and microwave engineering, can impair the signal quality and degrade the bit error rate of the link.

Agilent EEsof EDA has for years been proud to offer Advanced Design System (ADS) as the premier simulator of RF and microwave effects. RF and microwave engineers trust ADS to analyze their circuits and to help them mitigate the impairments encountered at these frequencies. Now, through continuous research and innovation, Agilent EEsof EDA offers three ADS bundles that put the applicable simulators, libraries, and capabilities into the hands of high-speed digital engineers.

Projected increase of clock frequencies

Source: ITRS 2004 Update to the SIA Roadmap
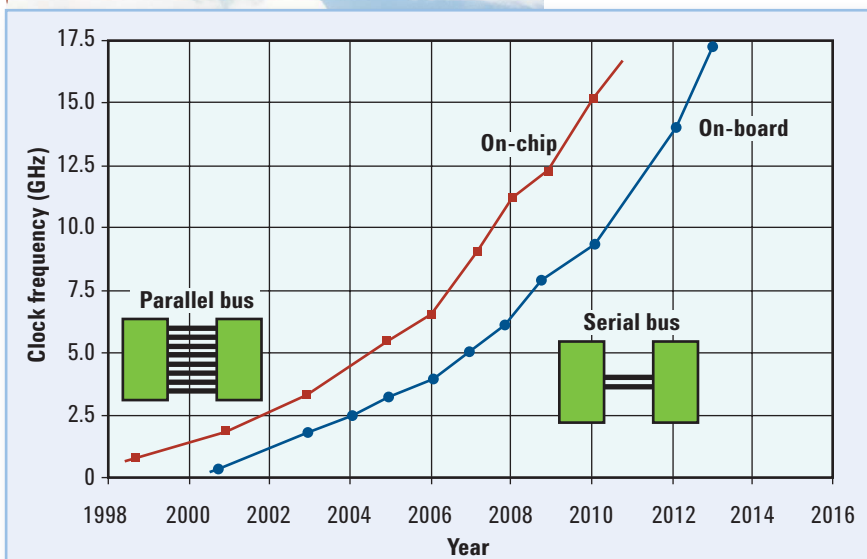
These bundles, listed in Table 1, provide the most complete serial link analysis for standards such as Infiniband, PCI Express, RapidIO, DDR, HDMI, and 10 gigabit/s Ethernet. They allow you to:

- Analyze complete chip-to-chip data links by co-simulating individual components, each at its most appropriate level of abstraction: link-, circuit- or physical-level.

- Import S-parameter accurately into transient simulation.

- Generate ultra-low bit error rate (BER) contours in seconds not days.

These capabilities result in dramatically reduced product design cycles.

The following sections highlight key features of the main modules that make up these bundles.

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| Element Model Number and Name	W2210 ADS Core, Transient Convolution Bundled	W2211 ADS Core, Transient Convolution, Layout, Momentum G2 Bundled
W2200 Advanced Design System (ADS) Core	●	●
W2302 Transient Convolution Element	●	●
W2321 Layout Element		●
W2341 Momentum G2 Element		●

ADS for high-speed digital design bundles come in different configurations to meet your design requirements.

Enhance your high speed digital bundle with these additional Elements:

- W2303 Verilog-A Element

- W2304 Verilog-AMS Element

- E8948 Momentum Turbo Element

- W2500 ADS Transient Convolution GT

- W2401 EMPro Core Environment

- W2342 Agilent FEM Simulator Element

- W2405 Agilent FDTD Simulator Element

- W1714 SystemVue AMI Modeling Kit

- W1713 SystemVue SerDes Model Library

This product configuration matrix illustrates the capabilities in each bundle.
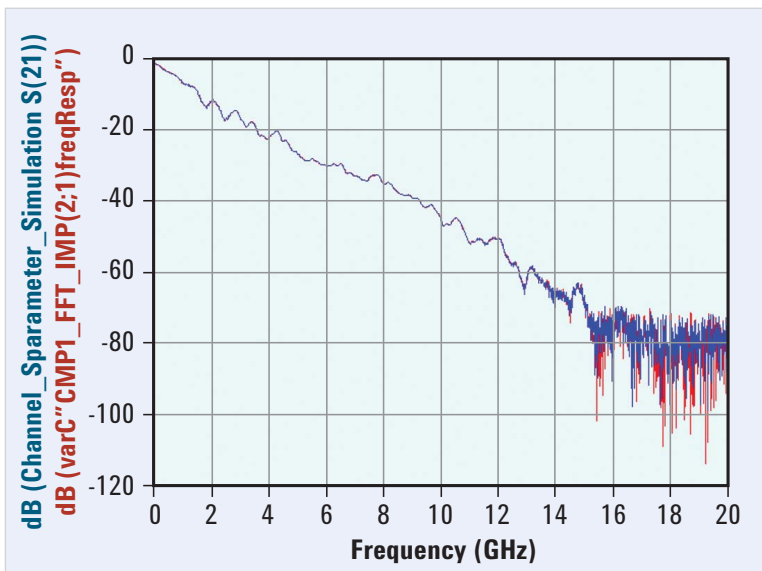
Comparison of 10 gigabit/second measured backplane S-parameters with "round trip" S-parameters derived from the model in ADS Transient Convolution Simulator.

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Transient Convolution Simulator

Chip-to-chip data links are found in almost all consumer and enterprise digital products produced today, from laptop computers to data center servers, telecom-munication switching centers and Internet routers.

At lower speeds, SPICE allowed designers to perform simulations using lumped-element models. But at today's multigigabit per second chip-to-chip data rates high-frequency and distributed effects such as impedance mismatch, reflections, crosstalk, skin effect, and dielectric loss come into play.

Accordingly, signal integrity engineers need to go beyond SPICE. The SPICE-like simulator portion of ADS Transient Convolution Element accommodates not only lumped-element models but also the distributed transmission line, S-parameter, and EM models that are essential to model high-speed PCB traces. The Transient Convolution Element is unique in that it is not simply a high performance point tool, but a set of capabilities integrated into the ADS platform. You can combine system-, circuit-, or EM-level models — each at the appropriate level of abstraction — into one simulation.

Multicore processor support and a new, high-capacity sparse matrix solver achieve a three-fold simulation speed improvement for traditional transient simulations and make this the industry's fastest signal integrity circuit simulator.
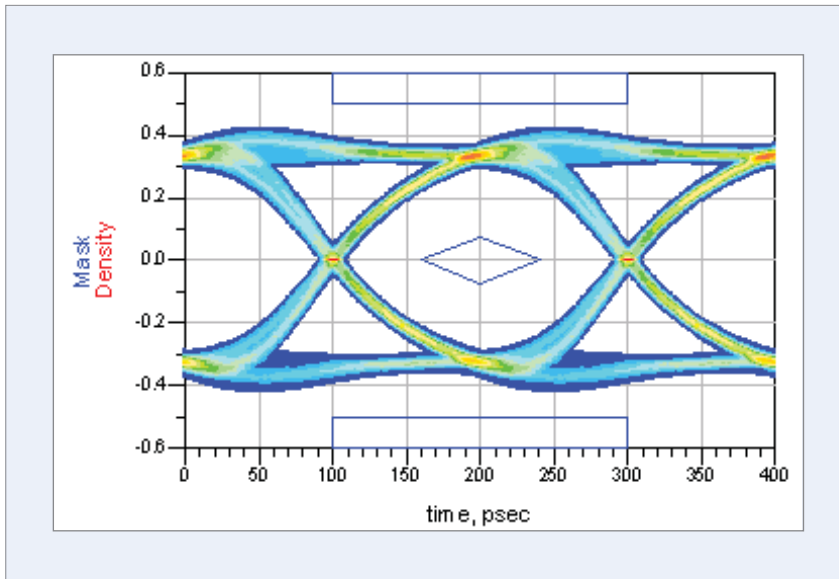
PCI Express Gen 2 eye diagram density contours with mask

Transient Convolution Element contains not only Transient Simulator but also many more capabilities for signal integrity including:

Convolution method (patent pending) to create causal and passive time-domain models from S-parameters. Unlike other tools, ADS Convolution handles challenging cases such a long or lossy transmission lines correctly. For analysis of power distribution networks (PDNs), the hybrid impulse/rational function mode yields the ultra fine frequency from DC to multigigahertz Channel Simulator with Bit-by-bit and Statistical modes (full details below) Eye Probe component that delivers eye diagram analysis including BER contour and bathtub display Eye mask utility with automatic violation checking Equalizer support with automatic tap optimization Ability to check cross-talk with multiple aggressors each at different data rates Memory bus compliance tool for the DDR3 standard Incorporate transceiver models complying with the IBIS I/O industry-standard (ANSI/EIA-656), including SERDES models built with the algorithmic modeling interface (AMI) Time-Domain Reflectometry tool Jitter decomposition using the proven EZJIT Plus algorithm used in Agilent instruments Broadband SPICE Model Generator, which lets you convert measured or simulated S-parameter models to lumped equivalent or pole zero representations

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Channel Simulator

Signal integrity engineers need to determine ultralow bit error rate (BER) contours for thousands of points in the design space in order to select the optimum set of characteristics for transmitter, channel, and receiver. Even with multicore and modern linear algebra, transient simulation still takes a prohibitively long time: more than a day for a million bits.

To meet this need, we've added two new modes that eliminate the need for long, transient simulations. It takes advantage of the fact that the traces, vias, bond wires, connectors, etc. of the channel are linear and time invariant ("LTI"). This fact lets you avoid the brute force approach of running the transient solver at every time step. You can determine ultralow BER contours in seconds not days. This enables very rapid and complete 'what if' design space exploration.

The table below compares the pros and cons of traditional transient with Channel Simulator in Bit-by-bit and Statistical modes.
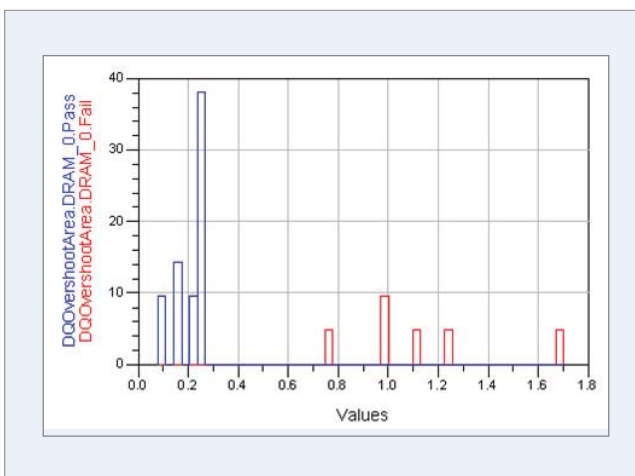
Pass-fail plot from the DDR3 compliance histogram measurements for DQ overshoot area

Comparison of traditional transient with channel simulator in bit-by-bit and statistical modes			
	Transient (SPICE-like) Simulator	**Channel Simulator, Bit-by-bit mod**	**Channel Simulator, Statistical mode**
Method	Modified nodal analysis of Kirchoff's current laws for every time step	Bit-by-bit superposition of step responses	Statistical calculations based on step response
Applicability	• Linear and non-linear channels • Finite, user-specified bit pattern • Adaptive or fixed equalizer taps	• LTI channels • Finite, user-specified bit pattern • Adaptive or fixed equalizer taps • Non-linear AMI Tx and Rx models	• LTI channels • Stochastic props of infinite bit pattern • Fixed equalizer taps • AMI Tx and Rx models (linearized)
BER floor in one minute simulation	$\sim 10^{-3}$	$\sim 10^{-6}$	$\sim 10^{-16}$
Typical megabit simulation time	25 hours	12 minutes	40 seconds

Decomposition of TDR/TDT measurements

Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) are measurement techniques that characterize a complex channel by sending an abrupt voltage step down a line and comparing the incident, transmitted, and reflected voltage waves. The shape and polarity of the transmission and reflection gives information about the position and nature of impedance changes at each discontinuity. Transient Convolution Simulator and the front panel TDR feature combine to form a highly accurate method for decomposing the measured TDR/TDT response into component behavior. By adjusting the component parameters to fit the composite response, you can reveal the cause of the underlying channel impairments.
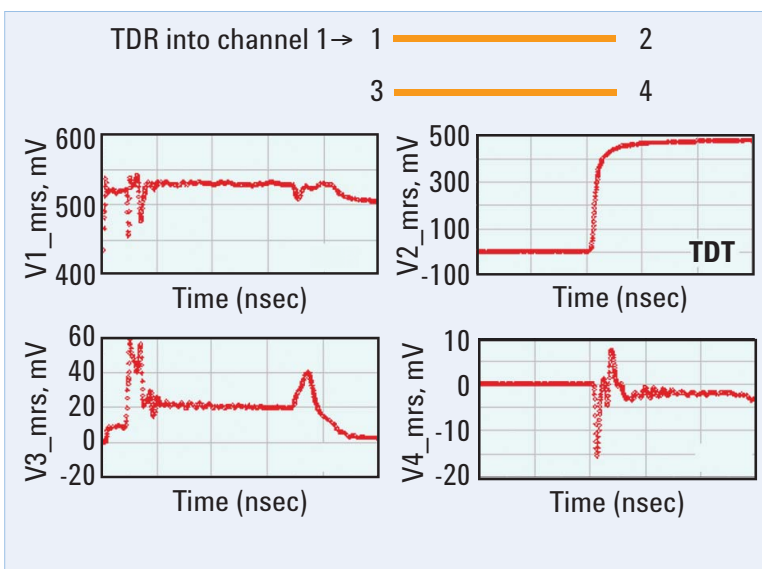
TDR/TDT response for a 2.5-Gbps differential channel

Broadband SPICE Model Generator

The Broadband SPICE Model Generator provides the capability to convert measured or simulated S-parameter models to lumped equivalent or pole zero representations. Lumped equivalent representations can be used with various types of SPICE simulators. It also gives you the ability to enforce passivity during broadband SPICE model extractions.
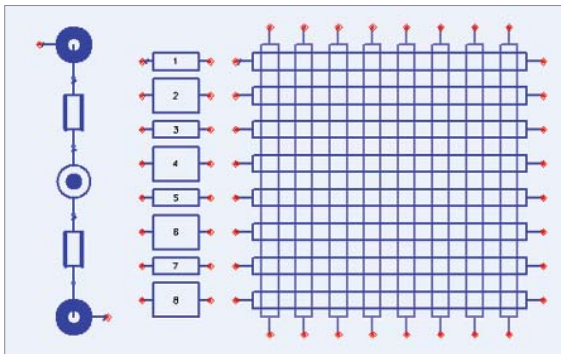
Multilayer Interconnect Models

This library contains up to 40 metal layers and 80 coupled lines. It offers an alternative trade off in simulation speed versus accuracy compared with the Momentum Planar EM simulator. The models run faster than Momentum, but Momentum is more accurate. The effects of impedance, loss, crosstalk, and delay are modeled with the simplified underlying 2-D electromagnetic field solver associated with these models.

The models include advance conductor surface roughness modeling, as well as a frequency-dependent dielectric loss.

Multilayer Interconnect Models have advantages over microstrip and stripline models, including a greater number of available coupled-line models, the ability to place them on any specific layer, and automatic computation of microstrip or stripline operations.
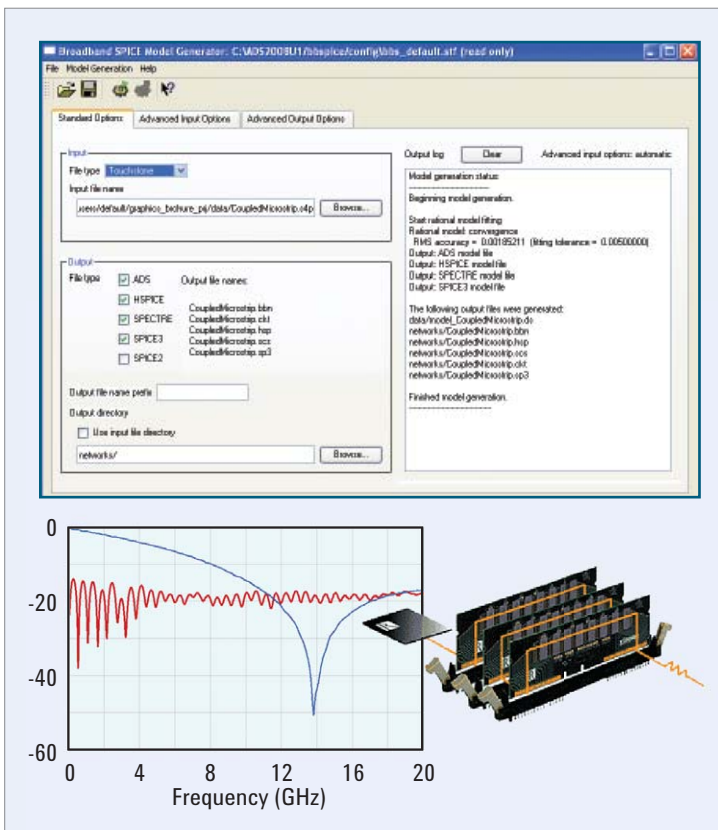

Broadband SPICE model overlays exactly with original S-parameters for a RambusTM device


Multilayer interconnect models

Jitter Decomposition

The Signal Integrity Verification Toolkit features powerful jitter analysis capabilities and provides excellent correlation between simulated and measured jitter components and BER measurements. The jitter algorithm in ADS is based on and is verified against the patented EZJIT Plus algorithm used in Agilent's test and measurement instruments.
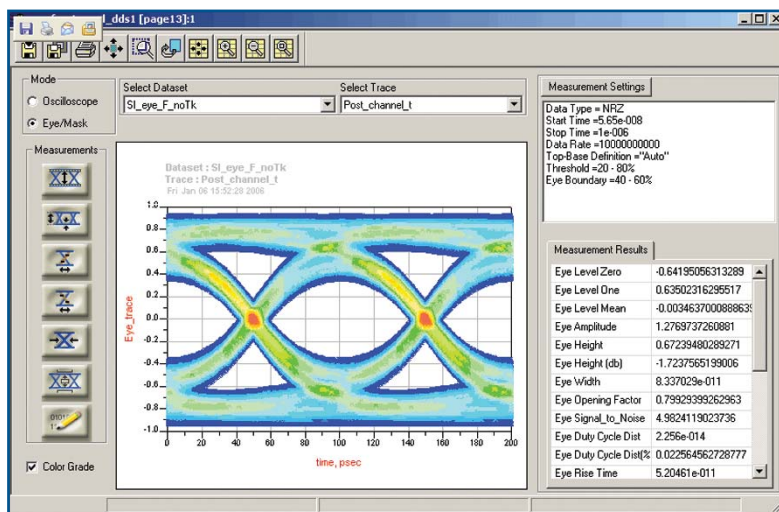
The eye diagram front panel in ADS allows you to calculate eye diagram parameters using an interface that is similar to that of Agilent instruments
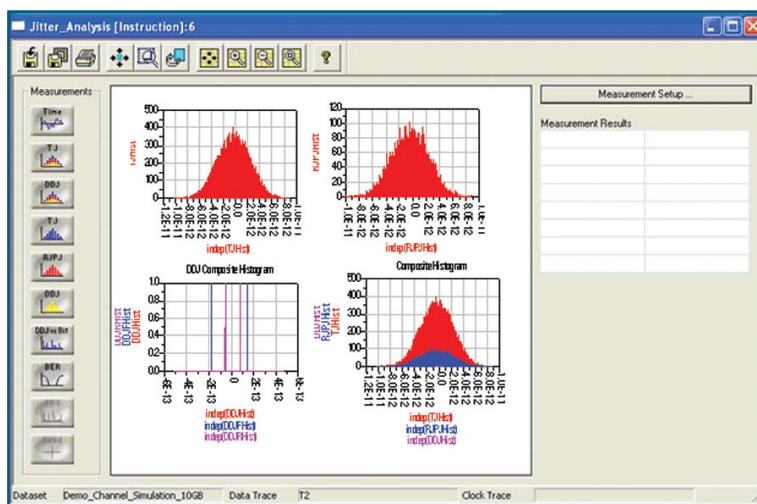

ADS provides powerful jitter analysis for analyzing all the random and deterministic jitter components present in a digital signal. It also provides accurate BER bathtub plots. The capability is based on patented EZJIT Plus technology, which is available in Agilent's real-time oscilloscopes.

IBIS I/O models

IBIS (I/O Buffer Information Specification) is an industry-standard specification for modeling input and outputs of digital circuits. Semiconductor vendors may create IBIS models for their parts and distribute them for use in any IBIS-compatible simulator. IBIS simulation provides faster simulation as compared with equivalent-circuit SPICE models. Using IBIS models, the nonlinear effects of integrated circuit I/O buffers can be modeled faster and more precisely, using vendor-supported information. Agilent representatives on the EIA IBIS committees contribute to and track these evolving standards, and help keep Agilent EEsof EDA tools up-to-date.

Recent advances include the addition of the algorithmic modeling interface (AMI) for vendor-specific IC models of SERDES signal processing blocks like pre-emphasis, equalization, and CDR.
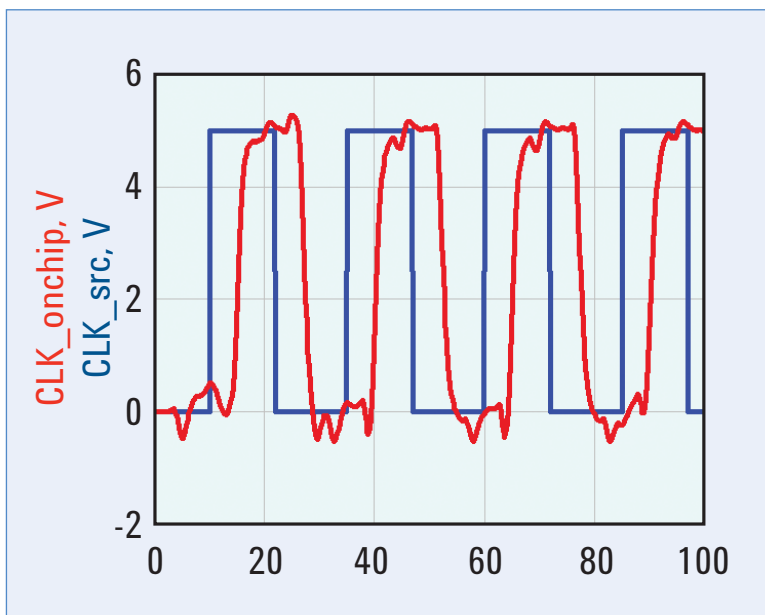
Comparison of received on-chip time-domain waveform and its source waveform.
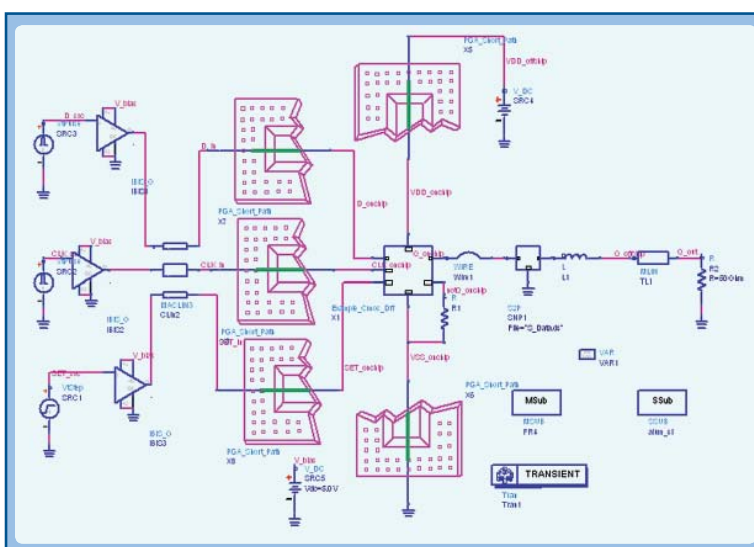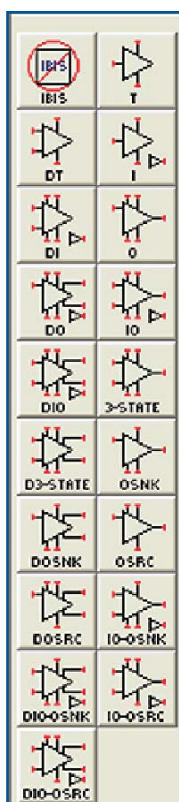
IBIS model palette and schematic showing time-domain simulation of IBIS models, package traces, and nonlinear transistor devices based on ASIC and S-parameter models.

Electromagnetic (EM) Simulators

Agilent EEsof EDA offers two EM simulators in ADS. These tools employ the method of moments and finite element method (FEM) methods.

Momentum G2 Element: The leading 3D-planar EM simulator

Momentum is a 3-D full-wave, multilayer electromagnetic (EM) simulator used for accurate interconnect analysis. It accepts arbitrary planar design geometries (including multi-layer traces and viaas) and accurately simulates complex 3-D EM effects including coupling and parasitics. Accurate EM simulation enables signal integrity designers to improve interconnect performance and increases confidence that the manufactured product will function as simulated.

Momentum RF is a the quasi-static mode of the Momentum EM engine that reduces simulation time, compared with Momentum's regular microwave solver technology, without sacrificing accuracy. It is particularly applicable to large and complex structures, and in case where full-wave field couplings (Ampère's law and the displacement current) need not be considered. Of course, conductive coupling is accounted for in both RF (quasi-static) and microwave modes (full-wave).

Electromagnetic/circuit co-simulation with layout components breaks down the barriers between electrical and physical analysis domains. The layout component technology allows ADS users to create layout components that can be used in both the physical and the schematic design views. Once artwork and ports are defined, the user can generate a layout component with the click of a button. Because Momentum is integrated into the ADS design flow, simulation setup times are reduced, and design productivity is increased.

Although Momentum is principally used for multilayer geometries it does also have a bond wire model that adds only one unknown per bond wire. Momentum also has the same frequency-dependent dielectric and conductor surface roughness capability as that the MLM library. Unlike previous generations of power integrity tools, Momentum make no assumption of solid power/ground planes can analyze PDNs with heavily perforated planes. The SI/PI Analyzer wizard lets you set up simulation in a snap using a net-based connection-oriented approach which augments the traditional polygon-by-polygon method.

FEM Element: An integrated, full 3D EM simulator

There are many types of components such as bondwire arcs and dielectric bricks that require 3-D electromagnetic analysis on non-multilayer geometries. FEM Element is ideal for this task. Designers can use ADS layout tools or import a layout from a third-party enterprise board tool such as Cadence Allegro or Mentor Expedition and simulate it using either Momentum (based on the method of moments) or FEM Element (based on the finite element method).

In addition to the ADS platform, our EMPro platform offers a full 3D CAD user interface that can export parameterized components to ADS. You can switch your FEM Element license back and forth between the ADS and EMPro user interfaces. We also offer a FDTD Element under the EMPro platform.
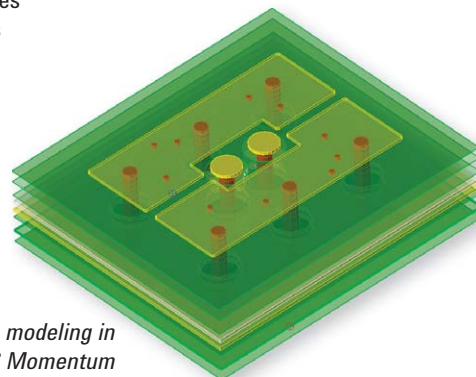
Trace and via modeling in ADS Momentum

# SERDES Modeling and IBIS AMI Model Generation with SystemVue

Two addons for our SystemVue ESL dataflow modeling tool offer serializer-deserializer (SerDes) models with (W1714 AMI Modeling Kit) or without (W1713 SerDes Model Library) automatic IBIS AMI model generation.

They let you optimize the signal processing blocks for your SerDes integrated circuit (IC) at the electronic system level (ESL). Once you've designed and optimized the algorithms, SystemVue automatically generates an IBIS AMI model that you can freely distribute to your customers as an 'executable datasheet' to help them design your chip into their system.

Use of SystemVue saves time, reduces engineering effort and accelerates the maturity of SerDes designs for next generation multigigabit transceiver (MGTs) in chip-to-chip serial links. They enable system architects, algorithm developers and hardware designers to investigate, implement and verify their SerDes signal

processing blocks in the presence of interconnect impairment models similar to those encountered in the systems the SerDes will be designed into. The libraries give the user piece of mind that their product meets or exceeds real-world performance requirements from the standards association of serial link like PCI Express, HDMI etc.

These addons provides measurement-hardened "golden reference" models that accelerate the SerDes design and verification process. The tool puts reliable Agilent measurement know-how at the front of the design process, where it improves the actual design, instead of only characterizing nonconformity after the fact. It can be used as a parameterized reference design to create test vectors for implemented blocks, or to fill in gaps to complete a fully-coded working chip-to-chip link, so that system-level performance can be continuously monitored.
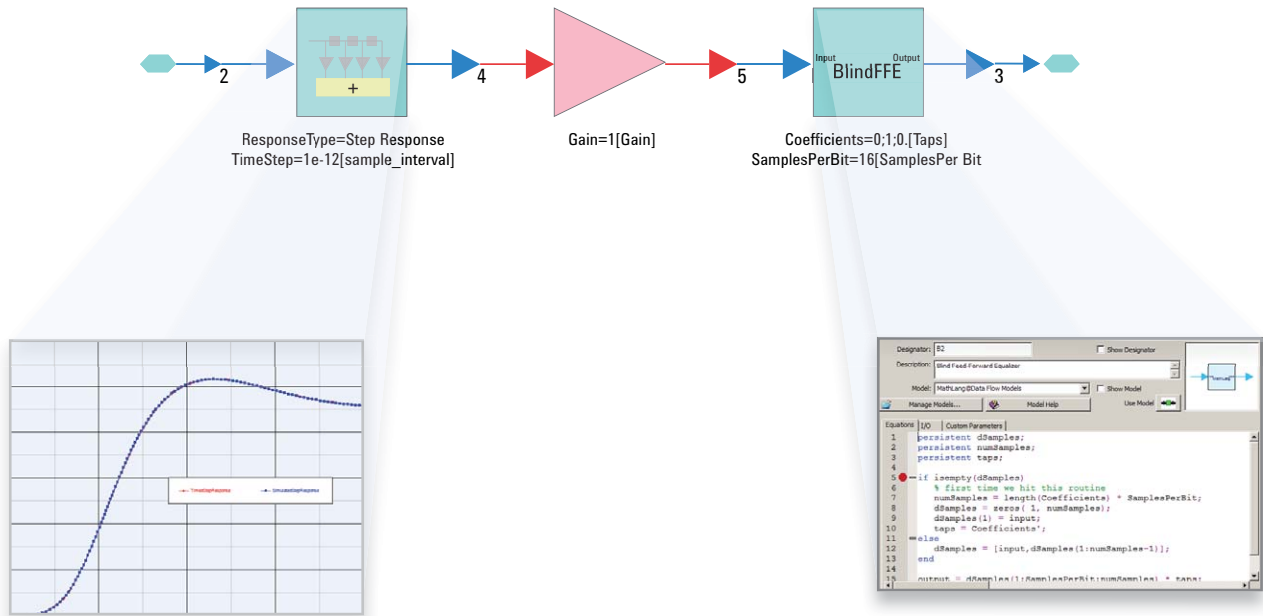
The SerDes model blocks can be specified in several way. The taps of the standard FIR block on the left were tuned so that the step response (blue) matches measured data (red). In contrast, the block on the right was created with custom code.

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www.agilent.com/find/eesof

For more information about applying Agilent's Advanced Design System to signal integrity challenges, visit:
www.agilent.com/find/signal-integrity

For information about Agilent's ADS Signal Integrity bundles, visit:
www.agilent.com/find/eesof-si-products

To request an evaluation of Agilent's Signal Integrity solutions, visit:
www.agilent.com/find/eesof-si-demo-software-request

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